WHAT IS CLAIMED IS:

1. An active matrix substrate comprising:

(a) a gate electrode layer, a gate insulating layer and an amorphous silicon semiconductor layer deposited in a substantially stacked fashion on a transparent insulating substrate, viewed from a direction normal to said transparent insulating substrate, to form a layered structure including a gate electrode, a gate wiring and a thin-film transistor area;

(b) a drain wiring formed on a first passivation film disposed on said substrate so as to cover said layered structure;

(c) a second passivation film formed as a layer overlying said drain wiring and said first passivation film;

(d) source/drain openings passing through said first passivation film and said second passivation film to reach said amorphous silicon semiconductor layer;

(e) an opening passing through said second passivation film to reach said drain wiring; and

(f) a wiring layer formed by a pixel electrode film disposed on said second passivation film, said wiring layer extending through said opening and openings for connection.

2. A vertical electrical field type active matrix substrate comprising:

(a) a gate electrode layer, a gate insulating layer and an amorphous silicon semiconductor layer deposited in a substantially stacked fashion on a transparent insulating

substrate, viewed from a direction normal to said transparent insulating substrate, to form a layered structure, including a gate electrode, a gate wiring and a thin-film transistor area;

(b) a drain wiring disposed on a first passivation film covering said layered structure; and

(c) a second passivation film formed as an overlying said drain wiring and said first passivation film,

(d) source/drain openings passing through said first passivation film and said second passivation film to reach said amorphous silicon semiconductor layer,

(e) an opening passing through said second passivation film to reach said drain wiring connection;

wherein

(f) a wiring layer extending through said drain opening to said drain wiring and a pixel electrode connected to said source opening are formed by a pixel electrode film disposed on said second passivation film;

and wherein

(g) said pixel electrode is provided with a storage capacitance unit comprised of the first and second passivation films sandwiched between the pixel electrode and an electrode layer formed as a co-layer as said gate electrode.

3. A vertical electrical field type active matrix substrate comprising:

(a) a gate electrode layer, a gate insulating layer and an

amorphous silicon semiconductor layer deposited in a substantially stacked fashion on a transparent insulating substrate, viewed from a direction normal to said transparent insulating substrate, to form a layered structure, including a gate electrode, a gate wiring and a thin-film transistor area;

(b) a drain wiring formed on a first passivation film disposed on said substrate so as to cover said layered structure;

(c) a second passivation film formed as a layer overlying said drain wiring and said first passivation film;

(d) source/drain openings passing through said first passivation film and said second passivation film to reach said amorphous silicon semiconductor layer; and

(e) an opening passing through said second passivation film to reach said drain wiring connection;

wherein

(f) a wiring layer extending through said drain opening to said drain wiring and a pixel electrode connected to said source opening are formed by a pixel electrode film disposed on said second passivation film;

and wherein

(g) said pixel electrode is provided with a storage capacitance unit comprised of the first passivation film sandwiched between said amorphous silicon semiconductor layer connected to said pixel electrode and an electrode layer formed as a co-layer as said gate electrode.

4. A lateral electrical field type active matrix substrate comprising:

(a) a gate electrode layer, a gate insulating layer and an amorphous silicon semiconductor layer deposited in a substantially stacked fashion on a transparent insulating substrate, viewed from a direction normal to said transparent insulating substrate, to form a layered structure, including a gate electrode, a gate wiring, a comb-shaped common electrode and a thin-film transistor area;

(b) a drain wiring formed on a first passivation film disposed on said substrate so as to cover said layered structure; and

(c) a second passivation film formed as a layer overlying said drain wiring and said first passivation film;

(d) source/drain openings passing through said first passivation film and said second passivation film to reach said amorphous silicon semiconductor layer, and

(e) an opening passing through said second passivation film to reach said drain wiring;

wherein

(f) a wiring layer extending through said drain opening to said drain wiring and a pixel electrode connected to said source opening are formed by a pixel electrode film disposed on said second passivation film.

5. A lateral electrical field type active matrix substrate

comprising:

(a) a gate electrode layer, a gate insulating layer and an amorphous silicon semiconductor layer deposited in a substantially stacked fashion on a transparent insulating substrate, viewed from a direction normal to said transparent insulating substrate, to form a layered structure, including a gate electrode, a gate wiring, a comb-shaped common electrode and a thin-film transistor area;

(b) a drain wiring formed on a first passivation film disposed on said substrate so as to cover said layered structure; and

(c) a second passivation film formed as a layer overlying said drain wiring and said first passivation film;

(d) source/drain openings passing through said first passivation film and said second passivation film to reach said amorphous silicon semiconductor layer, and

(e) an opening passing through said second passivation film to reach said drain wiring;

wherein

(f) a wiring layer extending through said drain opening to said drain wiring and a pixel electrode connected to said source opening are formed by a pixel electrode film, and

wherein

(g) said pixel electrode film is formed in a comb-shape on said first passivation film above said common electrode and is

covered by said second passivation film.

6. The active matrix substrate as defined in claim 1

wherein

said second passivation film has a substantially flattened surface, and wherein

said pixel electrode film is formed on said flattened surface.

7. The active matrix substrate as defined in claim 2

wherein

said second passivation film has a substantially flattened surface, and wherein

said pixel electrode film is formed on said flattened surface.

8. The active matrix substrate as defined in claim 3

wherein

said second passivation film has a substantially flattened surface, and wherein

said pixel electrode film is formed on said flattened surface.

9. The active matrix substrate as defined in claim 4

wherein

said second passivation film has a substantially flattened surface, and wherein

said pixel electrode film is formed on said flattened surface.

10. The active matrix substrate as defined in claim 5 wherein

said second passivation film has a substantially flattened surface, and wherein

said pixel electrode film is formed on said flattened surface.

11. The active matrix substrate as defined in claim 2 wherein said electrode layer is connected to said pixel electrode film through an opening provided in said first and/or second passivation films.

12. The active matrix substrate as defined in claim 3 wherein said electrode layer is connected to said pixel electrode film through an opening provided in said first and/or second passivation films.

13. The active matrix substrate as defined in claim 1 wherein said second passivation film is formed of a material having a high etching selectivity with respect to said amorphous silicon semiconductor layer and to said gate insulating film.

14. The active matrix substrate as defined in claim 2 wherein said second passivation film is formed of a material having a high etching selectivity with respect to said amorphous silicon semiconductor layer and to said gate insulating film.

15. The active matrix substrate as defined in claim 3

wherein said second passivation film is formed of a material having a high etching selectivity with respect to said amorphous silicon semiconductor layer and to said gate insulating film.

16. The active matrix substrate as defined in claim 4

wherein said second passivation film is formed of a material having a high etching selectivity with respect to said amorphous silicon semiconductor layer and to said gate insulating film.

17. The active matrix substrate as defined in claim 5

wherein said second passivation film is formed of a material having a high etching selectivity with respect to said amorphous silicon semiconductor layer and to said gate insulating film.

18. The active matrix substrate as defined in claim 13

wherein

said second passivation film is one of a silicon oxide film and a layered product of a silicon oxide film and an organic inter-layer film.

19. An active matrix substrate comprising:

(a) a gate electrode layer, a gate insulating film and an amorphous silicon semiconductor layer deposited in a substantially stacked fashion on an insulating substrate, viewed from a direction normal to said insulating substrate, to form a layered structure, including a gate electrode, a gate

wiring and a thin-film transistor area;

(b) a drain wiring formed on a passivation film covering said layered structure and said gate wiring;

(c) a black matrix formed on said passivation film at an area above said gate wiring, said layered structure and the drain wiring;

(d) a color layer or layers formed in a region surrounded by said black matrix;

(e) a planarized film formed to cover said passivation film and said black matrix; and

(f) source/drain openings passing through said passivation film and said planarized film to reach said amorphous silicon layer, and an opening passing through said black matrix and said planarized film to reach said drain wiring;

(g) a wiring layer connecting to said drain wiring layer through said drain opening by a pixel electrode film disposed on said planarized film.

20. The active matrix substrate as defined in claim 19 wherein

a pixel electrode connecting to said source opening is disposed by said pixel electrode film;

a capacitance electrode layer is disposed on said passivation film lying on said gate wiring; and wherein

said capacitance electrode layer is connected to said pixel electrode through openings formed in said black matrix and the planarized film.

21. The active matrix substrate as defined in claim 19 wherein said pixel electrode is branched from said gate wiring.

22. The active matrix substrate as defined in claim 1 wherein said pixel electrode film comprises a transparent electrode film; and wherein

an end of said pixel electrode is extended to above said gate wiring.

23. The active matrix substrate as defined in claim 1 wherein a n^+ layer doped with phosphorus is formed on a surface layer of an amorphous silicon semiconductor layer exposed by said opening, and wherein

said drain wiring or said pixel electrode is connected via said n^+ layer to said amorphous silicon semiconductor layer.

24. The active matrix substrate as defined in claim 2 wherein a n^+ layer doped with phosphorus is formed on a surface layer of an amorphous silicon semiconductor layer exposed by said opening, and wherein

said drain wiring or said pixel electrode is connected via said n^+ layer to said amorphous silicon semiconductor layer.

25. The active matrix substrate as defined in claim 3 wherein a n^+ layer doped with phosphorus is formed on a surface layer of an amorphous silicon semiconductor layer exposed by said opening, and wherein

said drain wiring or said pixel electrode is connected via said n^+ layer to said amorphous silicon semiconductor layer.

26. The active matrix substrate as defined in claim 4 wherein a n^+ layer doped with phosphorus is formed on a surface layer of an amorphous silicon semiconductor layer exposed by said opening, and wherein

said drain wiring or said pixel electrode is connected via said n^+ layer to said amorphous silicon semiconductor layer.

27. The active matrix substrate as defined in claim 5 wherein a n^+ layer doped with phosphorus is formed on a surface layer of an amorphous silicon semiconductor layer exposed by said opening, and wherein

said drain wiring or said pixel electrode is connected via said n^+ layer to said amorphous silicon semiconductor layer.

28. A method for producing an active matrix substrate comprising the steps of:

(a) layering a gate electrode layer, a gate insulating film and an a-Si layer in this order on a transparent insulating substrate and forming a gate electrode, a gate wiring and a thin-film transistor area, using a first mask;

(b) depositing a first passivation film and a drain electrode layer on said gate electrode, and removing said drain electrode layer lying in a preset area, using a second mask, to form a drain wiring;

(c) depositing a second passivation film above said drain wiring, forming openings, using a third mask, at preset positions in said amorphous silicon semiconductor layer passing

through said first and second passivation films for connection to source/drain electrodes as well as forming an opening, above said drain wiring, passing through said second passivation film; and

(d) depositing a transparent electrode layer as an overlying layer on said second passivation film and on and within said openings, to form a drain wiring connection connecting to an amorphous silicon layer exposed in said opening for said drain electrode, using a fourth mask, and to connect the amorphous silicon layer exposed in said opening for said source electrode to a pixel electrode comprised of said transparent electrode layer.

29. A method for producing an active matrix substrate comprising the steps of:

(a) layering a gate electrode layer, a gate insulating film and an a-Si layer in this order on a transparent insulating substrate to form a gate electrode, a gate wiring connection and a thin-film transistor area, using a first mask;

(b) depositing a first passivation film and a drain electrode layer on said gate electrode and removing said drain electrode metal layer lying in a preset area, using a second mask, to form a drain wiring and a storage capacitance electrode;

(c) depositing a second passivation film as an overlying layer of said drain wiring, forming openings, using a third mask, at preset positions in said amorphous silicon semiconductor

layer passing through said first and second passivation films for connection to source/drain electrodes, an opening above said drain wiring, passing through said second passivation film, and an opening for connection to said storage capacitance electrode; and

(d) depositing a transparent electrode layer as an overlying layer on said second passivation film and on and within said openings, to form a drain wiring connection connecting to an amorphous silicon layer exposed in an opening for said drain electrode, and a wiring connection for connection to said storage capacitance electrode, using a fourth mask, and connecting the amorphous silicon layer exposed in said opening for said source electrode to a pixel electrode comprised of said transparent electrode layer.

30. A method for producing an active matrix substrate comprising the steps of:

(a) layering a gate electrode layer, a gate insulating film and an a-Si layer in this order on a transparent insulating substrate and forming a gate electrode, a gate wiring, a common electrode and a thin-film transistor area, using a first mask;

(b) depositing a first passivation film and a drain electrode layer on said gate electrode and removing said drain electrode layer lying in a preset area, using a second mask, to form a drain wiring and pixel electrodes;

(c) depositing a second passivation film as an overlying

layer on said drain wiring, forming openings, using a third mask, at preset positions in said amorphous silicon semiconductor layer passing through said first and second passivation films for connection to source/drain electrodes, and an opening, above said drain wiring, passing through said second passivation film; and

(d) depositing a transparent electrode layer as an overlying layer on said second passivation film and on said openings, to form a drain wiring connection connecting to an amorphous silicon layer exposed in an opening for said drain electrode, using a fourth mask, and connecting the amorphous silicon layer exposed in said opening for said source electrode to a pixel electrode comprised of said transparent electrode layer.

31. The method for producing an active matrix substrate as defined in claim 22 wherein in step (a), said gate electrode is formed separate from said gate wiring, said common electrode being comb-shaped;

said pixel electrode being formed to comb shape in said step (b).

32. The method for producing an active matrix substrate as defined in claim 28 further comprising:

a step of substantially planarizing the surface of said second passivation film after step (c) and before step (d);

a step of forming said transparent electrode layer in step

(d) on the surface of said second passivation film.

33. The method for producing an active matrix substrate as defined in claim 28 wherein, in step (a), said gate insulating film and the amorphous silicon layer on said gate wiring are selectively removed, leaving

said gate insulating film and the amorphous silicon layer on said gate electrode.

34. A method for producing an active matrix substrate comprising the steps of:

(a) layering a gate electrode layer, a gate insulating film and an amorphous silicon layer in this sequence on an insulating substrate to form a gate electrode, a gate wiring and a thin film transistor area, using a first mask;

(b) depositing a passivation film and a drain electrode layer on said gate electrode and removing said drain electrode layer in a pre-set region, using a second mask, to form a drain wiring;

(c) forming a black matrix on said passivation film over said gate wiring and said drain wiring, and forming a color layer in a region surrounded by said black matrix on said passivation film;

(d) forming a planarized film covering said black matrix and the color layer;

(e) forming openings at pre-set positions in said amorphous silicon layer passing through said passivation film, black

matrix and the planarized film, using a third mask, for connection to source/drain electrodes, and also forming an opening, above said drain wiring, passing through said black matrix and said planarized film; and

(f) depositing a transparent electrode layer as an upper layer of said planarized film and said opening, forming a drain wiring connection connecting to a amorphous silicon layer exposed in an opening part of said drain electrode, using a fourth mask, and connecting the amorphous silicon layer exposed in an opening for said source electrode to a pixel electrode formed by said transparent electrode layer.

35. The method for producing an active matrix substrate as defined in claim 40 wherein,

in step (b), a storage capacitance electrode is formed on said passivation film lying on said gate wiring, simultaneously with formation of said drain wiring;

in step (e), an opening is formed passing through said black matrix and said planarized film above said capacitance electrode film, using a third mask; and

in step (f), said capacitance electrode film exposed to said opening and the pixel electrode made up of the transparent electrode layer are connected, using said fourth mask.

36. The method for producing an active matrix substrate as defined in claim 40, further comprising forming at least one color layer using at least one additional mask.

37. The method for producing an active matrix substrate as defined in claim 28 further comprising the steps of:

forming an ohmic contact layer within said openings as an overlying layer, following step (c) of forming the opening in said passivation film and before step (d) of forming said transparent electrode layer;

said transparent electrode layer being connected to said ohmic contact layer.

38. The method for producing an active matrix substrate as defined in claim 28

wherein

said second passivation film is formed of a material having a high etching selectivity with respect to said amorphous silicon semiconductor layer and the gate insulating film.

39. The method for producing an active matrix substrate as defined in claim 44

wherein said second passivation film is one of a silicon oxide film and a composite laminate layer of a silicon oxide film and an organic inter-layer film.

40. A liquid crystal display device comprising the active matrix substrate as defined in claim 1.

41. A liquid crystal display device comprising the active matrix substrate as defined in claim 2.

42. A liquid crystal display device comprising the active matrix substrate as defined in claim 3.

43. A liquid crystal display device comprising the active matrix substrate as defined in claim 4.

44. A liquid crystal display device comprising the active matrix substrate as defined in claim 5.